multiplexer circuitry, coupled to the output driver circuitry, to provide the first and second portions of data to the output driver circuitry.

17 ~~167~~. (Amended) The memory controller of claim 16 ~~166~~ [further including: multiplexer circuitry coupled to the output driver circuitry,] wherein:

in response to the rising edge [first] transition of the external clock signal, the multiplexer circuitry provides [couples the first portion of] data to [an input of] the output driver circuitry; and

in response to the falling edge [second] transition of the external clock signal, the multiplexer circuitry provides [couples the second portion of] data to [the input of] the output driver circuitry.

In claim 168, line 5, delete "the input of".

In claim 169, line 4, delete "input of the".

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22 ~~172~~. (Amended) A memory controller for controlling a synchronous memory device, the memory controller comprising:

output driver circuitry to output data wherein:

the output driver circuitry outputs a first portion of data in response to a first external clock signal; and

the output driver circuitry outputs a second portion of data in response to a second external clock signal;and

multiplexer circuitry coupled to the output driver circuitry, to provide the first and second portions of data to the output driver circuitry.

~~173~~ 23. (Amended) The memory controller of claim ~~172~~ 22, further including:

multiplexer circuitry coupled to the output driver circuitry,] wherein:

in response to the first external clock signal, the multiplexer circuitry provides [couples the first portion of] data to [an input of] the output driver circuitry; and

in response to the second external clock signal, the multiplexer circuitry provides [couples the second portion of] data to [the input of] the output driver circuitry.

In claim 174, line 5, delete "the input of".

In claim 175, line 4, delete "input of the".